Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of testing an electronic memory device that includes a control logic circuit portion, a matriz array of memory cell, and storage circuitry integrated together on a semiconductor substrate, the method comprising:

loading test data and/or instructions into ~~a~~ the control logic circuit portion ~~associated with a matrix array of memory cells and storage circuitry~~ using a test operation control device, temporarily, ~~for said control logic,~~ said test operation control device being external of, and temporarily connected to, said memory device; and

testing the semiconductor device.

2. (Currently Amended) A method according to claim 1, wherein said test operation control device comprises a matrix cell array external to the memory device, and wherein the testing step comprises loading using the external matrix cell array to simulate the matrix array of memory cells of the semiconductor device.

3. (Currently Amended) A method according to claim 1, wherein said test operation control device comprises a control logic external to the memory device, and wherein the testing step comprises simulating the control logic circuit of the semiconductor device using the external control logic.

4. (Currently Amended) A method according to claim 1, ~~characterized in that~~ further comprising temporarily connecting the test operation control device to said memory

device ~~said temporary connection is established~~ through data pins and address pins of the memory device, as well as over respective connecting buses.

5. (Currently Amended) A method according to claim 1, wherein said memory array is ~~control logic is incorporated in~~ a non-volatile memory ~~device~~array.

6. (Currently Amended) A control device for testing an electronic memory devices having ~~provided with~~ a matrix array of memory cells and a control logic circuit portion associated with the memory cell array, as well as ~~with~~ circuitry associated with said control logic, the control device comprising a memory unit external of and detachably connectable~~ed~~ to the memory device, the memory unit configured to operate in substitution of the memory cell array during testing.

7. (Original) A device according to claim 6, wherein the detachable connection is established through data pins and address pins of the memory device.

8. (Original) A device according to claim 6, wherein said external memory unit is a non-volatile type.

9. (Original) A device comprising:

an internal memory array integrated onto a semiconductor substrate;

a control logic circuit integrated onto the semiconductor substrate; and

a test control device, external to the semiconductor substrate, having a circuit for simulating the internal memory array to permit testing of the control logic circuit in isolation from the internal memory array.

10. (Currently Amended) The device of claim 9, wherein the test control device includes a circuit for simulating the control logic circuit, the device being detachably ~~connected~~ connectable to the semiconductor substrate.

11. (Original) The device of claim 10, wherein the circuit for simulating the internal memory array and the circuit for simulating the control logic circuit are integrated into one test device.

12. (Original) The device of claim 9, wherein the circuit for simulating the internal memory array is an external memory array.

13. (Original) The device of claim 9, wherein the circuit for simulating the internal memory array comprises a software program in an external memory executed by a testing circuit.

14. (Original) A method for testing a memory array integrated, with a control logic circuit, onto a semiconductor substrate, comprising:

simulating the control logic circuit, using an external connected circuit;

performing test operations with the memory array and the external connected circuit; and

observing interactions between the memory array and the external connected circuit.

~~14~~15. (Currently Amended) A method for testing a control logic circuit integrated, with a memory array, onto a semiconductor substrate, comprising:

simulating the memory array, using an external connected circuit;

performing test operations with the control logic circuit and the external connected circuit; and

observing interactions between the control logic circuit and the external connected circuit.

16. (New) A device, comprising:

a semiconductor substrate;

a memory array formed on the substrate;

a control logic circuit formed on the substrate and configured to control operation of the memory array under normal operating conditions; and

bypass circuitry formed on the substrate configured to permit substitution of an external memory array for the purpose of testing the control logic circuit, separate from the memory array formed on the substrate.

17. (New) The device of claim 16, further comprising bypass circuitry formed on the substrate configured to permit substitution of an external control logic circuit for the purpose of testing the memory array, separate from the control logic circuit formed on the substrate.

18. (New) The device of claim 16 wherein the bypass circuitry comprises an instruction set programmed into the control logic circuit.